

## 1M x 4-Bit Dynamic RAM (Hyper Page Mode (EDO) version)

HYB 514405BJ/BJL-50/-60/-70

### Preliminary Information

- 1 048 576 words by 4-bit organization
- 0 to 70 °C operating temperature
- Hyper Page Mode - EDO
- Performance:

		-50	-60	-70	
$t_{RAC}$	$\overline{RAS}$ access time	50	60	70	ns
$t_{CAC}$	$\overline{CAS}$ access time	13	15	20	ns
$t_{AA}$	Access time from address	25	30	35	ns
$t_{RC}$	Read/Write cycle time	89	104	124	ns
$t_{HPC}$	Hyper page mode (EDO) cycle time	20	25	30	ns

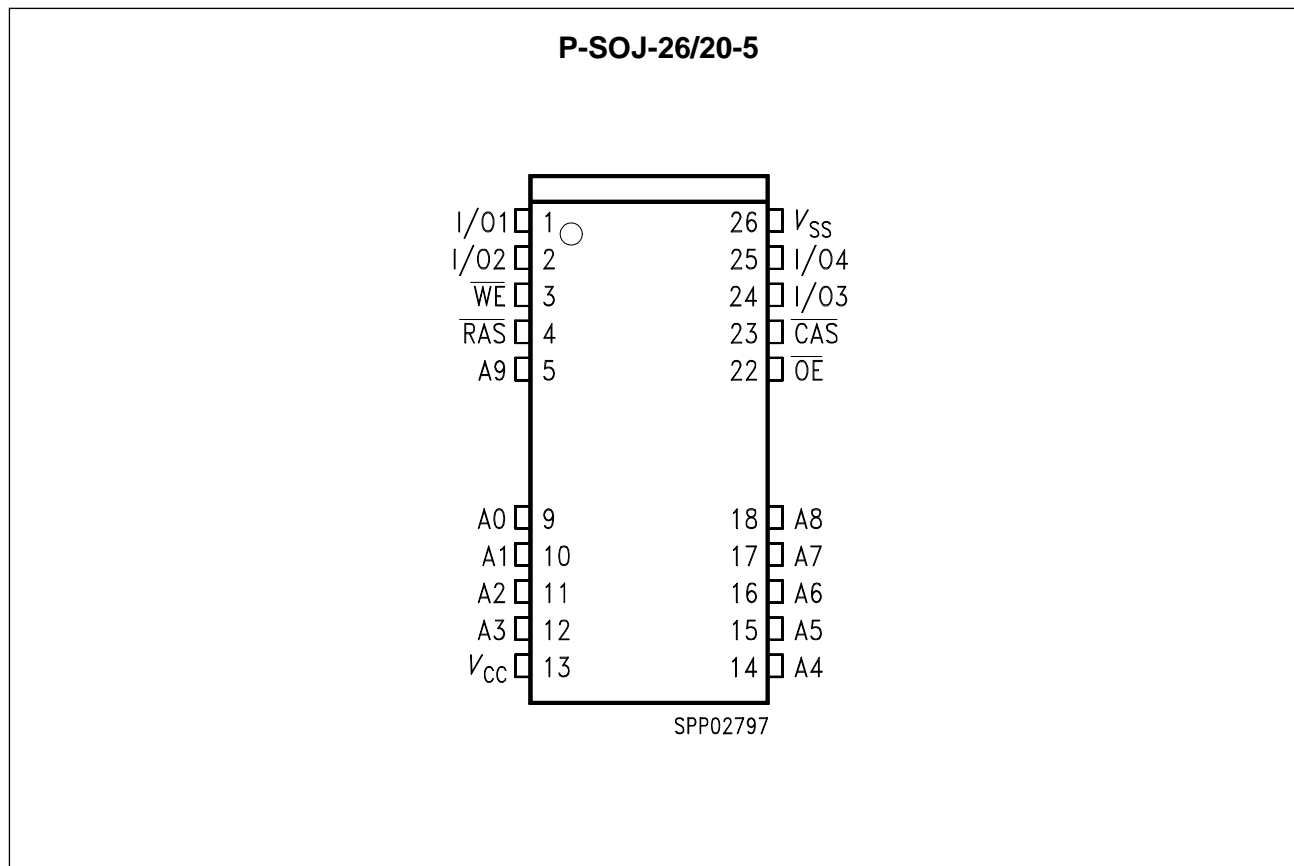
- Single + 5 V ( $\pm 10\%$ ) supply
- Low power dissipation  
max. 660 mW active (-50 version)  
max. 605 mW active (-60 version)  
max. 550 mW active (-70 version)
- Standby power dissipation:  
11 mW max.standby (TTL)  
5.5 mW max.standby (CMOS)  
1.1 mW max.standby (CMOS) for Low Power Version
- Read, write, read-modify write,  $\overline{CAS}$ -before- $\overline{RAS}$  refresh,  $\overline{RAS}$ -only refresh, hidden refresh and test mode capability
- All inputs and outputs TTL-compatible
- 1024 refresh cycles / 16 ms
- 1024 refresh cycles / 128 ms for Low Power Version
- Plastic Packages: P-SOJ-26/20-5 with 300 mil width

The HYB 514405BJ is the new generation dynamic RAM organized as 1 048 576 words by 4-bit. The HYB 514405BJ utilizes CMOS silicon gate process as well as advances circuit techniques to provide wide operation margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514405BJ to be packed in a standard plastic P-SOJ-26/20 package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented feature include single + 5 V ( $\pm 10\%$ ) power supply, direct interfacing with high performance logic device families.

### Ordering Information

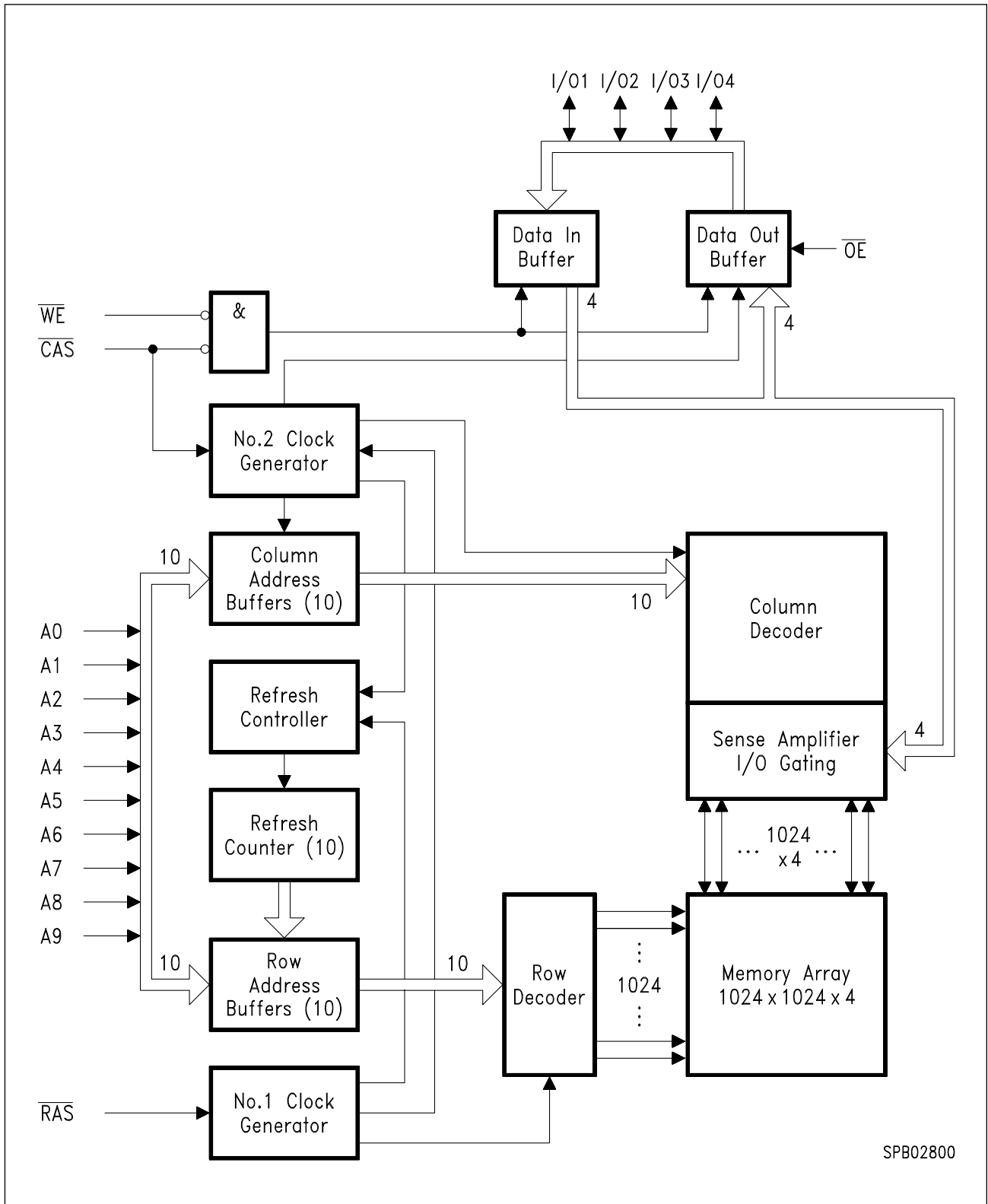
Type	Ordering Code	Package	Descriptions
HYB 514405BJ-50	Q67100-Q2116	P-SOJ-26/20-5	EDO-DRAM (access time 50 ns)
HYB 514405BJ-60	Q67100-Q2118	P-SOJ-26/20-5	EDO-DRAM (access time 60 ns)
HYB 514405BJ-70	Q67100-Q2120	P-SOJ-26/20-5	EDO-DRAM (access time 70 ns)
HYB 514405BJL-50	on request	P-SOJ-26/20-5	Low Power EDO-DRAM (access time 50 ns)
HYB 514405BJL-60	on request	P-SOJ-26/20-5	Low Power EDO-DRAM (access time 60 ns)
HYB 514405BJL-70	on request	P-SOJ-26/20-5	Low Power EDO-DRAM (access time 70 ns)

### Pin Configuration (top view)



### Pin Names

A0-A9	Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Read/Write Input
$\overline{\text{OE}}$	Output Enable
I/O1 - I/O4	Data Input/Output
$V_{\text{CC}}$	Power Supply (+ 5 V)
$V_{\text{SS}}$	Ground (0 V)
N.C.	No Connection



Block Diagram

### Absolute Maximum Ratings

Operating temperature range .....	0 to 70 °C
Storage temperature range.....	- 55 to + 150 °C
Input/output voltage .....	- 1 to + 7 V
Power Supply voltage .....	- 1 to + 7 V
Data out current (short circuit) .....	50 mA

**Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC Characteristics

$T_A = 0$  to 70 °C,  $V_{SS} = 0$  V,  $V_{CC} = 5$  V  $\pm$  10 %,  $t_T = 2$  ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	$V_{ih}$	2.4	$V_{CC} + 0.5$	V	1)
Input low voltage	$V_{il}$	- 1.0	0.8	V	1)
Output high voltage ( $I_{OUT} = - 5$ mA)	$V_{oh}$	2.4	-	V	1)
Output low voltage ( $I_{OUT} = 4.2$ mA)	$V_{ol}$	-	0.4	V	1)
Input leakage current, any input ( $0$ V < $V_{in}$ < 7, all other input = 0 V)	$I_{l(L)}$	- 10	10	$\mu$ A	1)
Output leakage current (DO is disabled, $0 < V_{OUT} < V_{CC}$ )	$I_{o(L)}$	- 10	10	$\mu$ A	1)
Average $V_{CC}$ supply current -50 version -60 version -70 version	$I_{CC1}$	-	120 110 100	mA	2) 3)4)
Standby $V_{CC}$ supply current (RAS = CAS = WE = $V_{ih}$ )	$I_{CC2}$	-	2	mA	-
Average $V_{CC}$ supply current during $\overline{\text{RAS}}$ -only refresh cycles -50 version -60 version -70 version	$I_{CC3}$	-	120 110 100	mA	2)4)
Average $V_{CC}$ supply current during hyper page mode(EDO) operation -50 version -60 version -70 version	$I_{CC4}$	-	100 90 80	mA	2) 3)4)
Standby $V_{CC}$ supply current (RAS = CAS = WE = $V_{CC} - 0.2$ V)	$I_{CC5}$	-	1 200	mA $\mu$ A	1) L-version

### DC Characteristics (cont'd)

$T_A = 0$  to  $70$  °C,  $V_{SS} = 0$  V,  $V_{CC} = 5$  V  $\pm$  10 %,  $t_T = 2$  ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average $V_{CC}$ supply current during CAS before RAS refresh mode -50 version -60 version -70 version	$I_{CC6}$	–	120 110 100	mA	2)4)
For Low Power Version only: Battery backup current (average power supply current in battery backup mode): (CAS = CAS before RAS cycling or 0.2 V, $\overline{WE} = V_{CC} - 0.2$ V or 0.2 V, A0 to A10 = $V_{CC} - 0.2$ V or 0.2 V; DI = $V_{CC} - 0.2$ V or 0.2 V or open, $t_{RC} = 125$ $\mu$ s, $t_{RAS} = t_{RAS}$ min = 1 $\mu$ s)	$I_{CC7}$	–	250	$\mu$ A	–

### AC Characteristics 5)6)

$T_A = 0$  to  $70$  °C,  $V_{CC} = 5$  V  $\pm$  10 %,  $t_T = 2$  ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		

### Common Parameters

Random read or write cycle time	$t_{RC}$	89	–	104	–	124	–	ns	
RAS precharge time	$t_{RP}$	35	–	40	–	50	–	ns	
RAS pulse width	$t_{RAS}$	50	10k	60	10k	70	10k	ns	
CAS pulse width	$t_{CAS}$	8	10k	10	10k	12	10k	ns	
Row address setup time	$t_{ASR}$	0	–	0	–	0	–	ns	
Row address hold time	$t_{RAH}$	8	–	10	–	10	–	ns	
Column address setup time	$t_{ASC}$	0	–	0	–	0	–	ns	
Column address hold time	$t_{CAH}$	8	–	10	–	12	–	ns	
RAS to CAS delay time	$t_{RCD}$	12	37	14	45	14	53	ns	
RAS to column address delay time	$t_{RAD}$	10	25	12	30	12	35	ns	
RAS hold time	$t_{RSH}$	13		15	–	17	–	ns	

### AC Characteristics (cont'd) <sup>5)6)</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 5$  V  $\pm$  10 %,  $t_T = 2$  ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
CAS hold time	$t_{CSH}$	50		60	–	70	–	ns	
CAS to RAS precharge time	$t_{CRP}$	5	–	5	–	5	–	ns	
Transition time (rise and fall)	$t_T$	1	50	1	50	1	50	ns	7
Refresh period	$t_{REF}$	–	16	–	16	–	16	ms	
Refresh period for L-version	$t_{REF}$	–	128	–	128	–	128	ms	

### Read Cycle

Access time from $\overline{RAS}$	$t_{RAC}$	–	50	–	60	–	70	ns	8, 9
Access time from $\overline{CAS}$	$t_{CAC}$	–	13	–	15	–	17	ns	8, 9
Access time from column address	$t_{AA}$	–	25	–	30	–	35	ns	8,10
$\overline{OE}$ access time	$t_{OEA}$	–	13	–	15	–	17	ns	
Column address to $\overline{RAS}$ lead time	$t_{RAL}$	25	–	30	–	35	–	ns	
Read command setup time	$t_{RCS}$	0	–	0	–	0	–	ns	
Read command hold time	$t_{RCH}$	0	–	0	–	0	–	ns	11
Read command hold time referenced to $\overline{RAS}$	$t_{RRH}$	0	–	0	–	0	–	ns	11
CAS to output in low-Z	$t_{CLZ}$	0	–	0	–	0	–	ns	8
Output buffer turn-off delay	$t_{OFF}$	0	13	0	15	0	17	ns	12
Output buffer turn-off delay from $\overline{OE}$	$t_{O EZ}$	0	13	0	15	0	17	ns	12
Data to $\overline{CAS}$ low delay	$t_{DZC}$	0	–	0	–	0	–	ns	13
Data to $\overline{OE}$ low delay	$t_{DZO}$	0	–	0	–	0	–	ns	13
CAS high to data delay	$t_{CDD}$	10	–	13	–	15	–	ns	14
$\overline{OE}$ high to data delay	$t_{ODD}$	10	–	13	–	15	–	ns	14

### Write Cycle

Write command hold time	$t_{WCH}$	8	–	10	–	10	–	ns	
Write command pulse width	$t_{W P}$	8	–	10	–	10	–	ns	
Write command setup time	$t_{WCS}$	0	–	0	–	0	–	ns	15

### AC Characteristics (cont'd) <sup>5)6)</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 5$  V  $\pm$  10 %,  $t_T = 2$  ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
Write command to $\overline{\text{RAS}}$ lead time	$t_{RWL}$	13	–	15	–	17	–	ns	
Write command to $\overline{\text{CAS}}$ lead time	$t_{CWL}$	13	–	15	–	17	–	ns	
Data setup time	$t_{DS}$	0	–	0	–	0	–	ns	16
Data hold time	$t_{DH}$	8	–	10	–	12	–	ns	16

### Read-modify-Write Cycle

Read-write cycle time	$t_{RWC}$	118	–	138	–	162	–	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	$t_{RWD}$	64	–	77	–	89	–	ns	15
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	$t_{CWD}$	27	–	32	–	36	–	ns	15
Column address to $\overline{\text{WE}}$ delay time	$t_{AWD}$	39	–	47	–	54	–	ns	15
$\overline{\text{OE}}$ command hold time	$t_{OEH}$	10	–	13	–	15	–	ns	

### Hyper Page Mode (EDO) Cycle

Hyper page mode (EDO) cycle time	$t_{HPC}$	20	–	25	–	30	–	ns	
$\overline{\text{CAS}}$ precharge time	$t_{CP}$	8	–	10	–	10	–	ns	
Access time from $\overline{\text{CAS}}$ precharge	$t_{CPA}$	–	27	–	32	–	37	ns	7
Output data hold time	$t_{COH}$	5	–	5	–	5	–	ns	
$\overline{\text{RAS}}$ pulse width in hyper page mode	$t_{RAS}$	50	200k	60	200k	70	200k	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{RAS}}$ Delay	$t_{RHCP}$	27	–	32	–	37	–	ns	

### Hyper Page Mode (EDO) Read-modify-Write Cycle

Hyper page mode (EDO) read-write cycle time	$t_{PRWC}$	58	–	68	–	77	–	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$	$t_{CPWD}$	41	–	49	–	56	–	ns	



### AC Characteristics (cont'd) <sup>5)6)</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 5$  V  $\pm$  10 %,  $t_T = 2$  ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		

### $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle

CAS setup time	$t_{CSR}$	10	–	10	–	10	–	ns	
CAS hold time	$t_{CHR}$	10	–	10	–	10	–	ns	
RAS to $\overline{\text{CAS}}$ precharge time	$t_{RPC}$	5	–	5	–	5	–	ns	
Write to $\overline{\text{RAS}}$ precharge time	$t_{WRP}$	10	–	10	–	10	–	ns	
Write hold time referenced to RAS	$t_{WRH}$	10	–	10	–	10	–	ns	

### CAS-before-RAS Counter Test Cycle

CAS precharge time ( $\overline{\text{CAS}}$ -before-RAS counter test cycle)	$t_{CPT}$	35	–	40	–	40	–	ns	
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### Test Mode

Write command setup time	$t_{WTS}$	10	–	10	–	10	–	ns	
Write command hold time	$t_{WTH}$	10	–	10	–	10	–	ns	

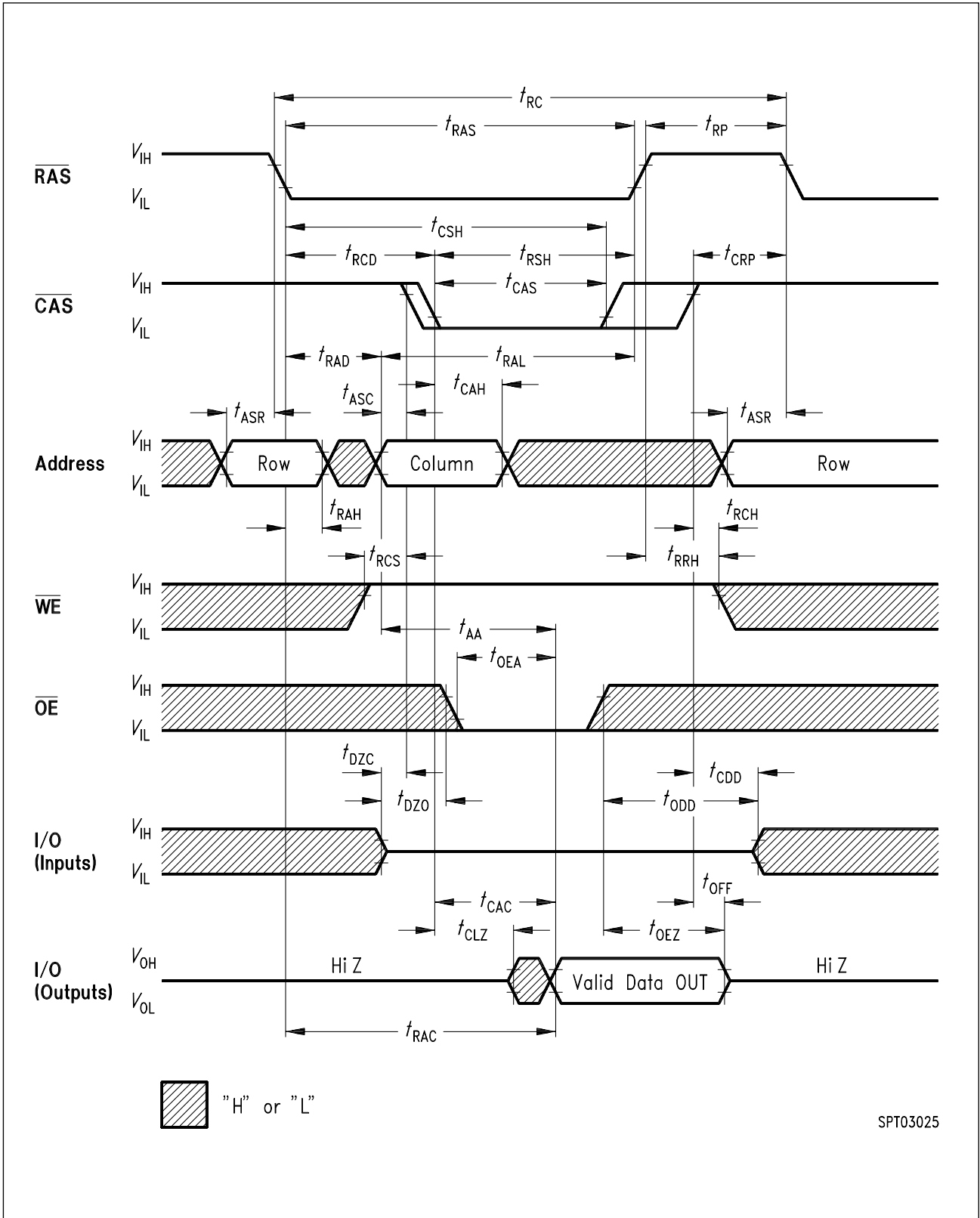
### Capacitance

$T_A = 0$  to  $70$  °C;  $V_{CC} = 5$  V  $\pm$  10 %;  $f = 1$  MHz

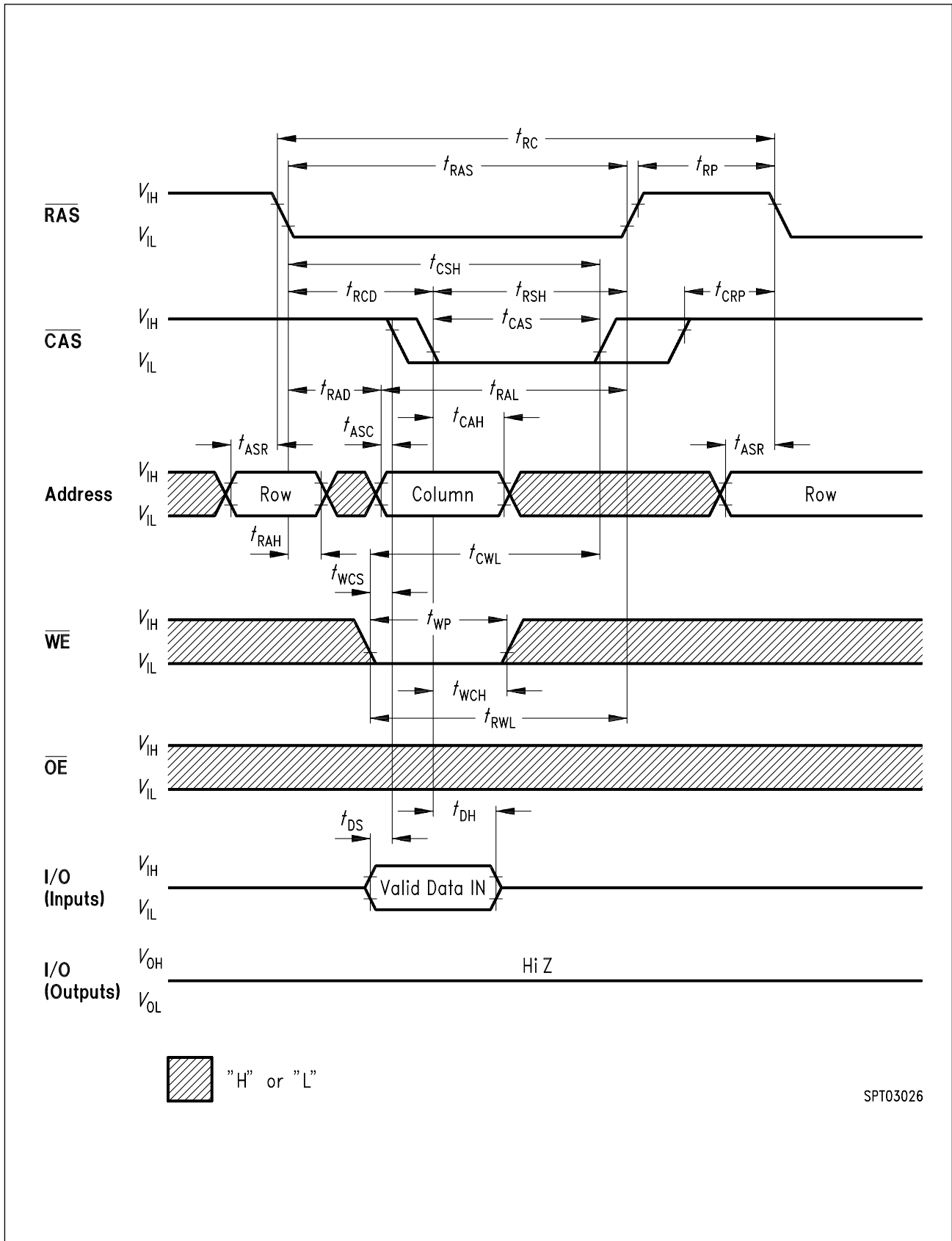
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9)	$C_{i1}$	–	5	pF
Input capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ )	$C_{i2}$	–	7	pF
Output capacitance (IO1 to IO4)	$C_{io}$	–	7	pF

**Notes:**

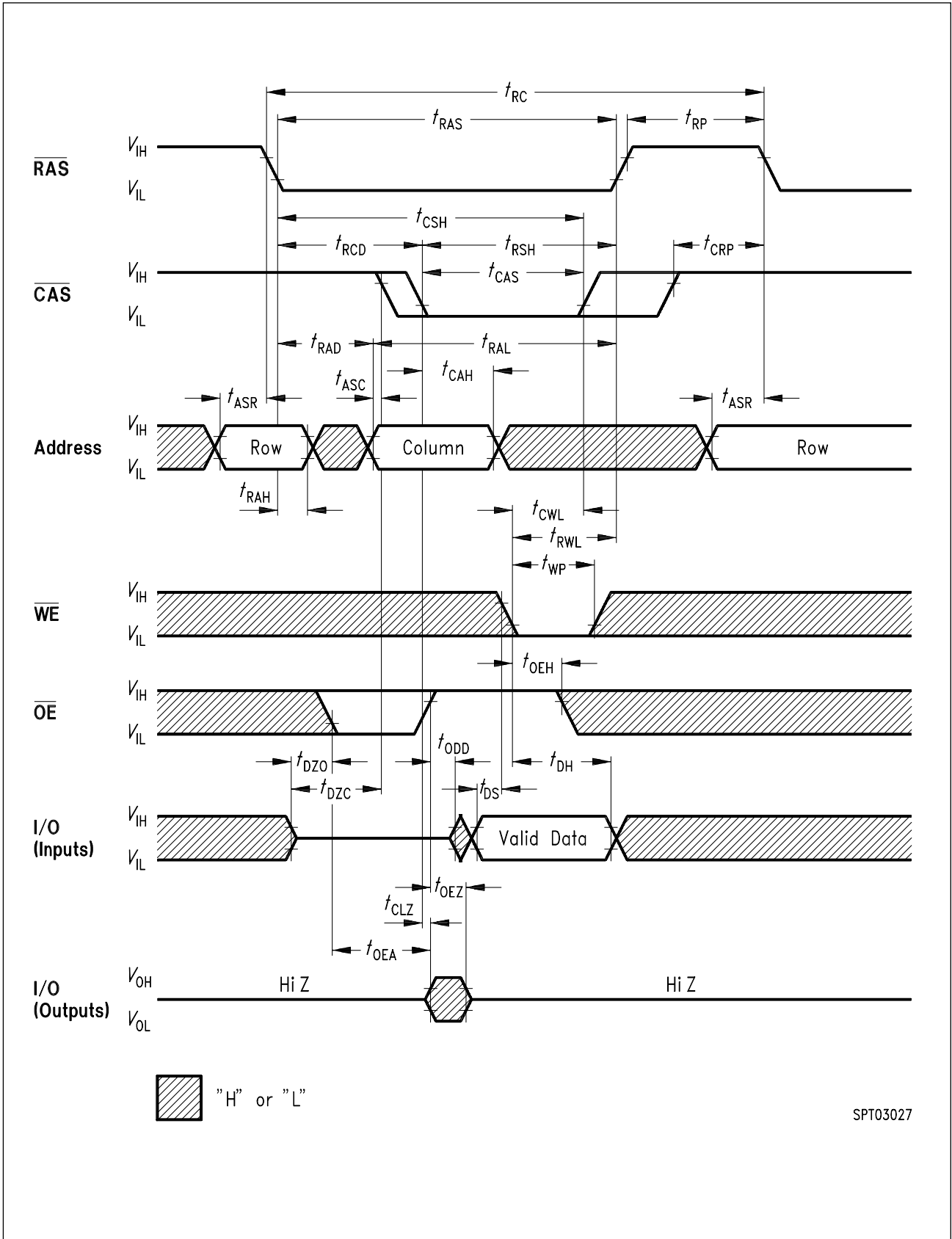
- 1) All voltages are referenced to  $V_{SS}$ .
- 2)  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC6}$  depend on cycle rate.
- 3)  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
- 4) Address can be changed once or less while  $RAS = V_{il}$ . In case of  $I_{CC4}$  it can be changed once or less during a hyper page mode (EDO) cycle
- 5) An initial pause of 200  $\mu s$  is required after power-up followed by 8  $\overline{RAS}$  cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.
- 6) AC measurements assume  $t_T = 2$  ns.
- 7)  $V_{IH (min.)}$  and  $V_{IL (max.)}$  are reference levels for measuring timing of input signals. Transition times are also measured between  $V_{IH}$  and  $V_{IL}$ .
- 8) Measured with the specified current load and 100 pF at  $V_{ol} = 0.8$  V and  $V_{oh} = 2.0$  V. Access time is determined by the latter of  $t_{RAC}$ ,  $t_{CAC}$ ,  $t_{AA}$ ,  $t_{CPA}$ ,  $t_{OEA}$ .  $t_{CAC}$  is measured from tristate.
- 9) Operation within the  $t_{RCD (max.)}$  limit ensures that  $t_{RAC (max.)}$  can be met.  $t_{RCD (max.)}$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD (max.)}$  limit, then access time is controlled by  $t_{CAC}$ .
- 10) Operation within the  $t_{RAD (max.)}$  limit ensures that  $t_{RAC (max.)}$  can be met.  $t_{RAD (max.)}$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD (max.)}$  limit, then access time is controlled by  $t_{AA}$ .
- 11) Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
- 12)  $t_{OFF (max.)}$ ,  $t_{OEZ (max.)}$  define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels.  $t_{OFF}$  is referenced from the rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ , whichever occurs last.
- 13) Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.
- 14) Either  $t_{CDD}$  or  $t_{ODD}$  must be satisfied.
- 15)  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} > t_{WCS (min.)}$ , the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if  $t_{RWD} > t_{RWD (min.)}$ ,  $t_{CWD} > t_{CWD (min.)}$  and  $t_{AWD} > t_{AWD (min.)}$ , the cycle is a read-write cycle and I/O will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.
- 16) These parameters are referenced to the  $\overline{CAS}$  leading edge in early write cycles and to the  $\overline{WE}$  leading edge in read-write cycles.



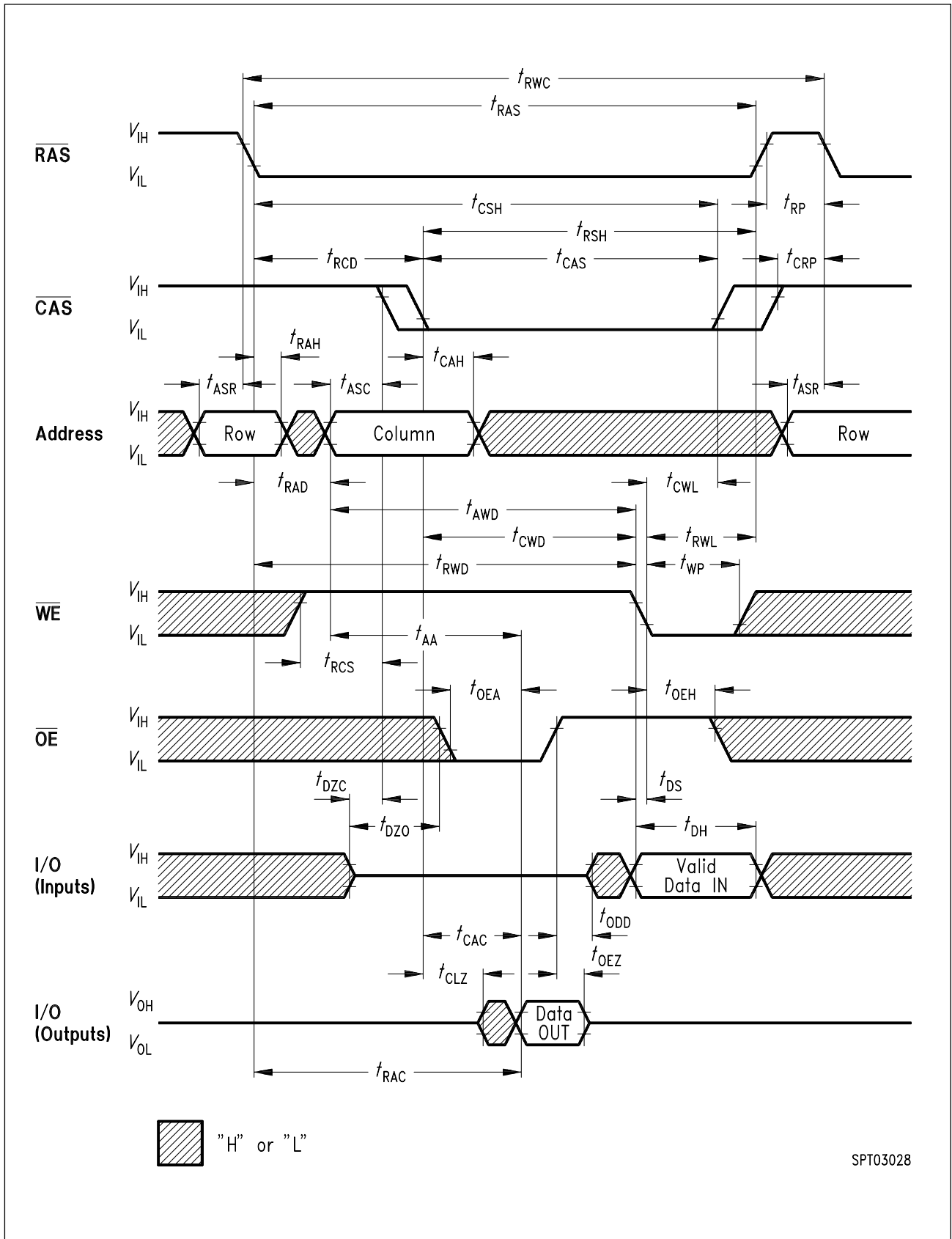
Read Cycle



### Write Cycle (Early Write)



Write Cycle ( $\overline{OE}$  Controlled Write)



### Read-Write (Read-Modify-Write) Cycle

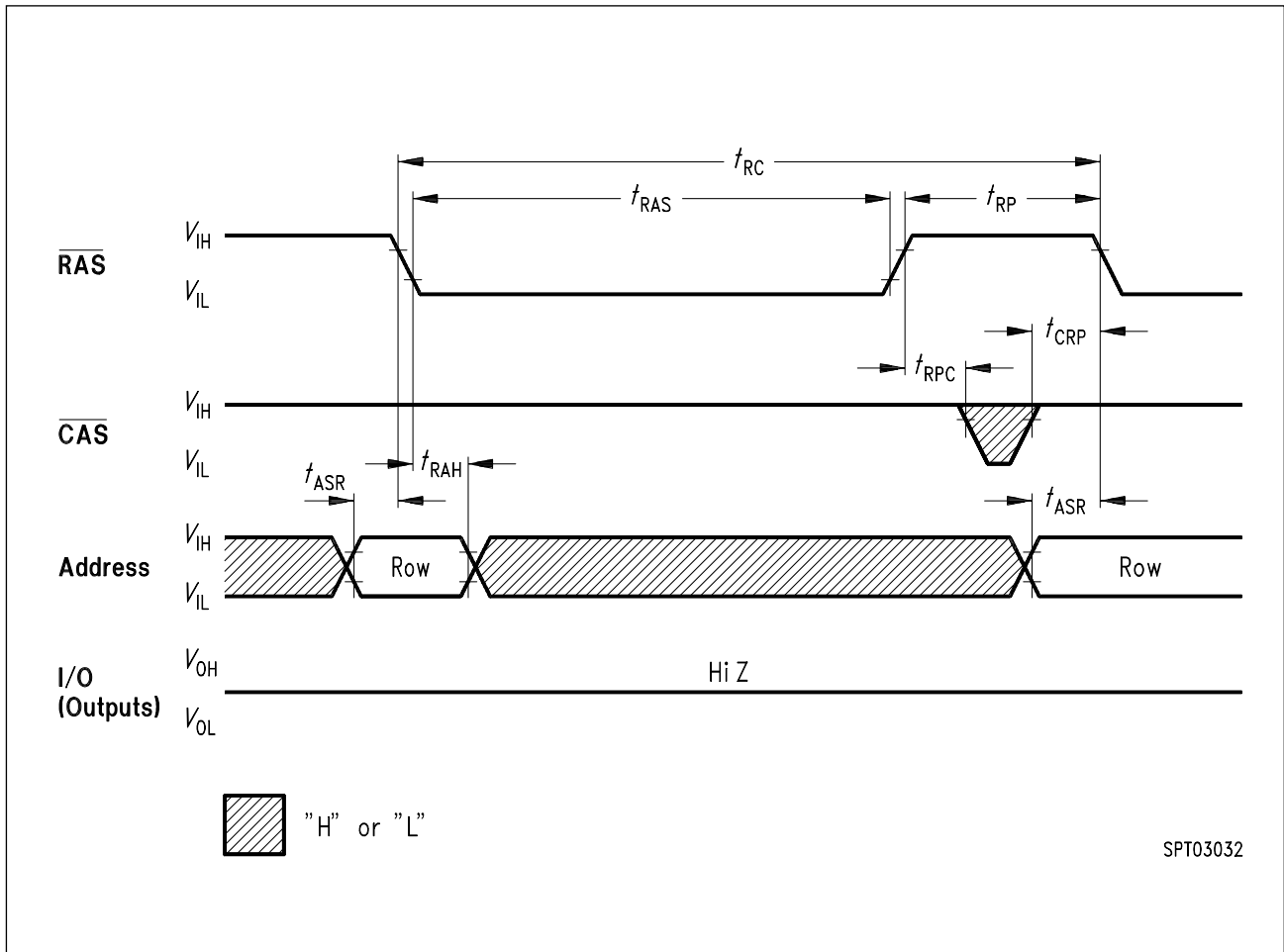




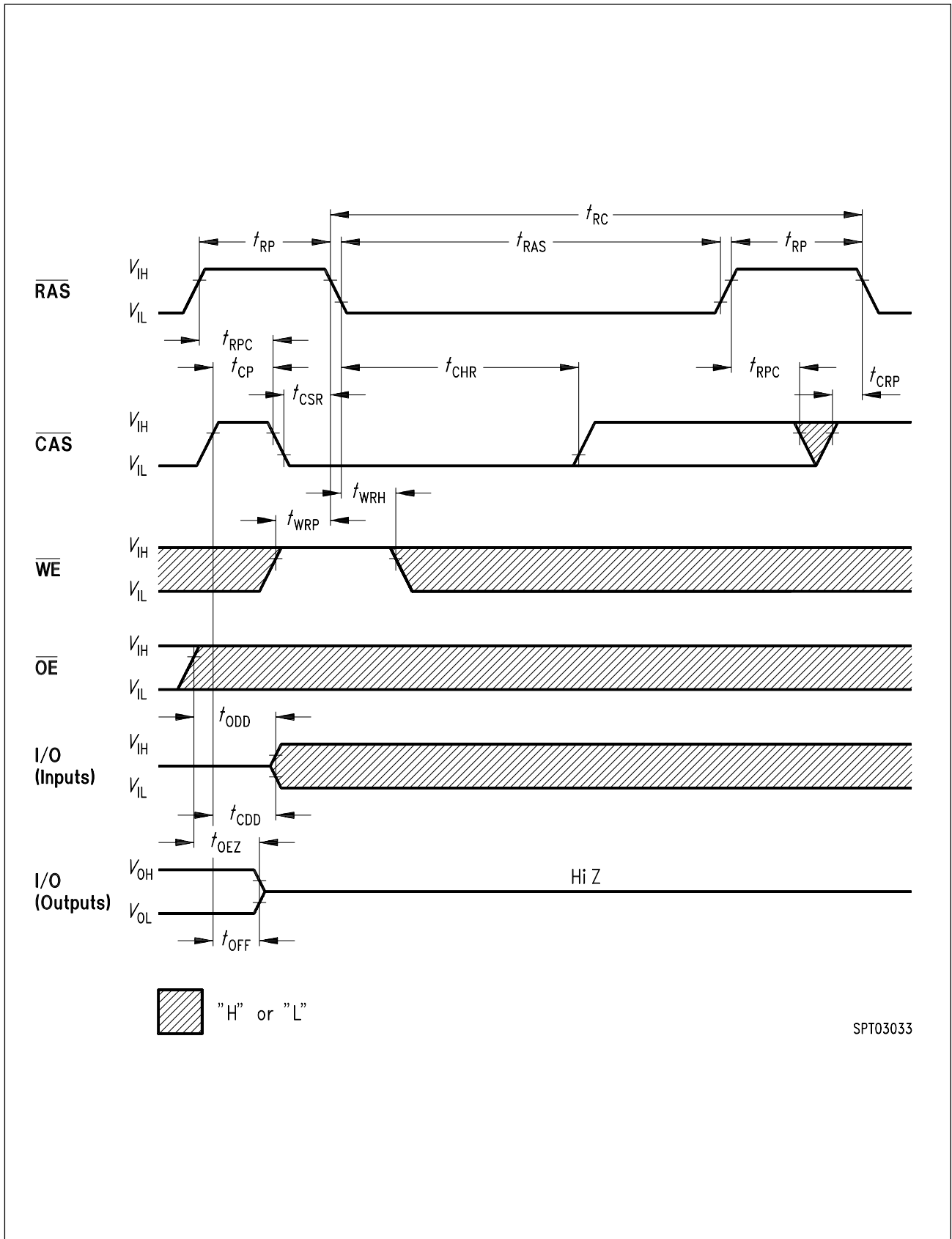






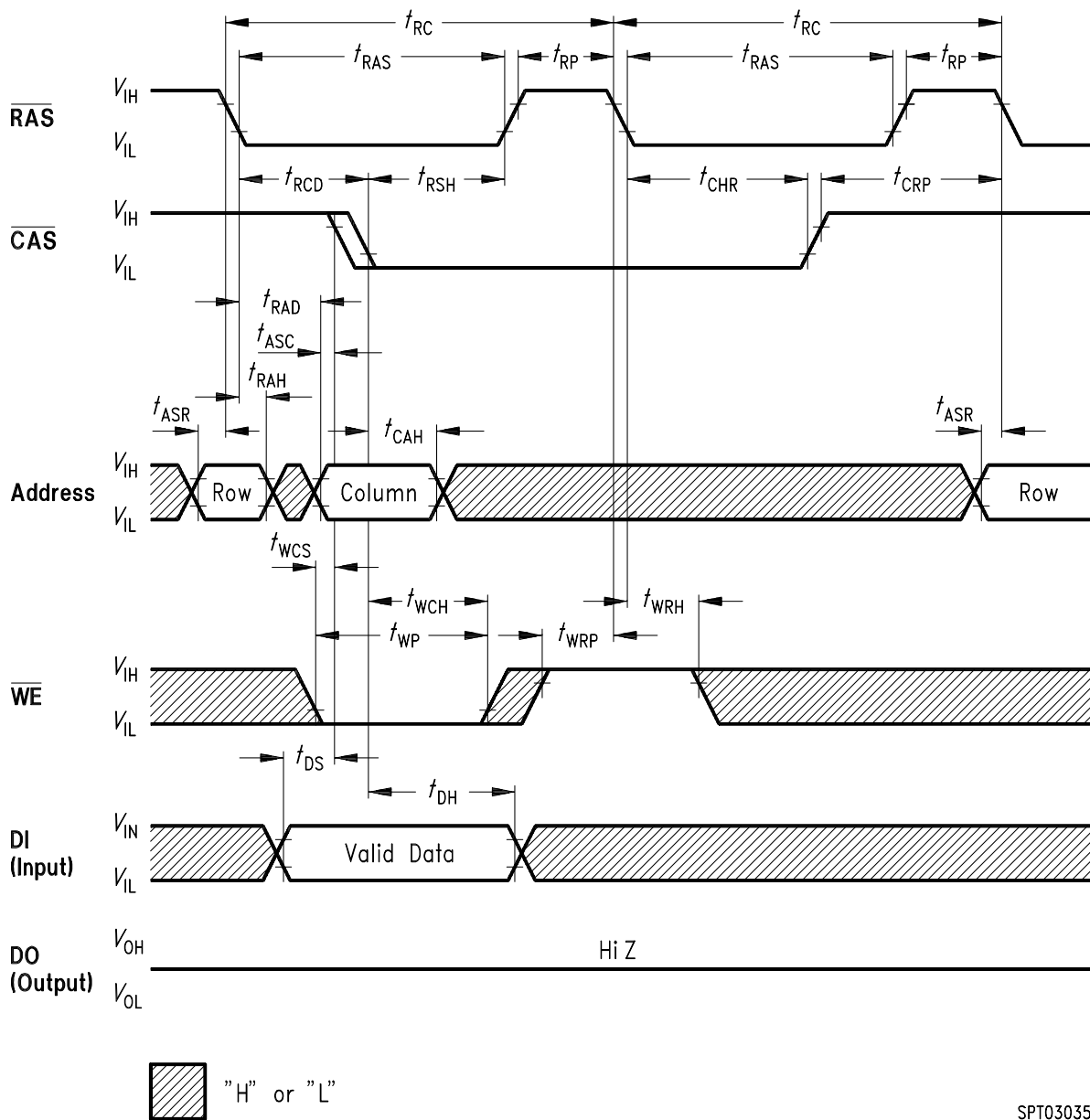


### $\overline{\text{RAS}}$ -Only Refresh Cycle



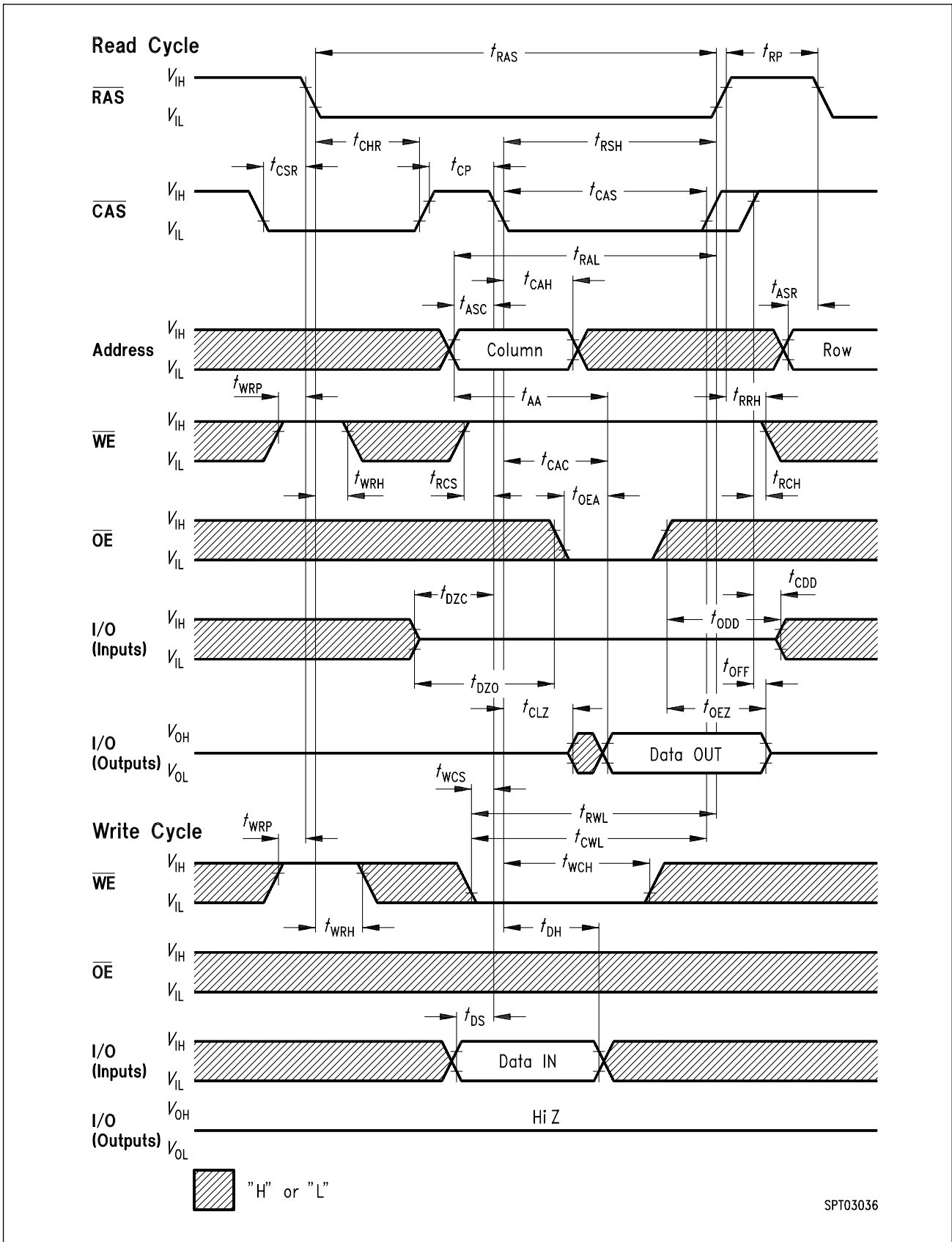
**CAS-Before-RAS Refresh Cycle**



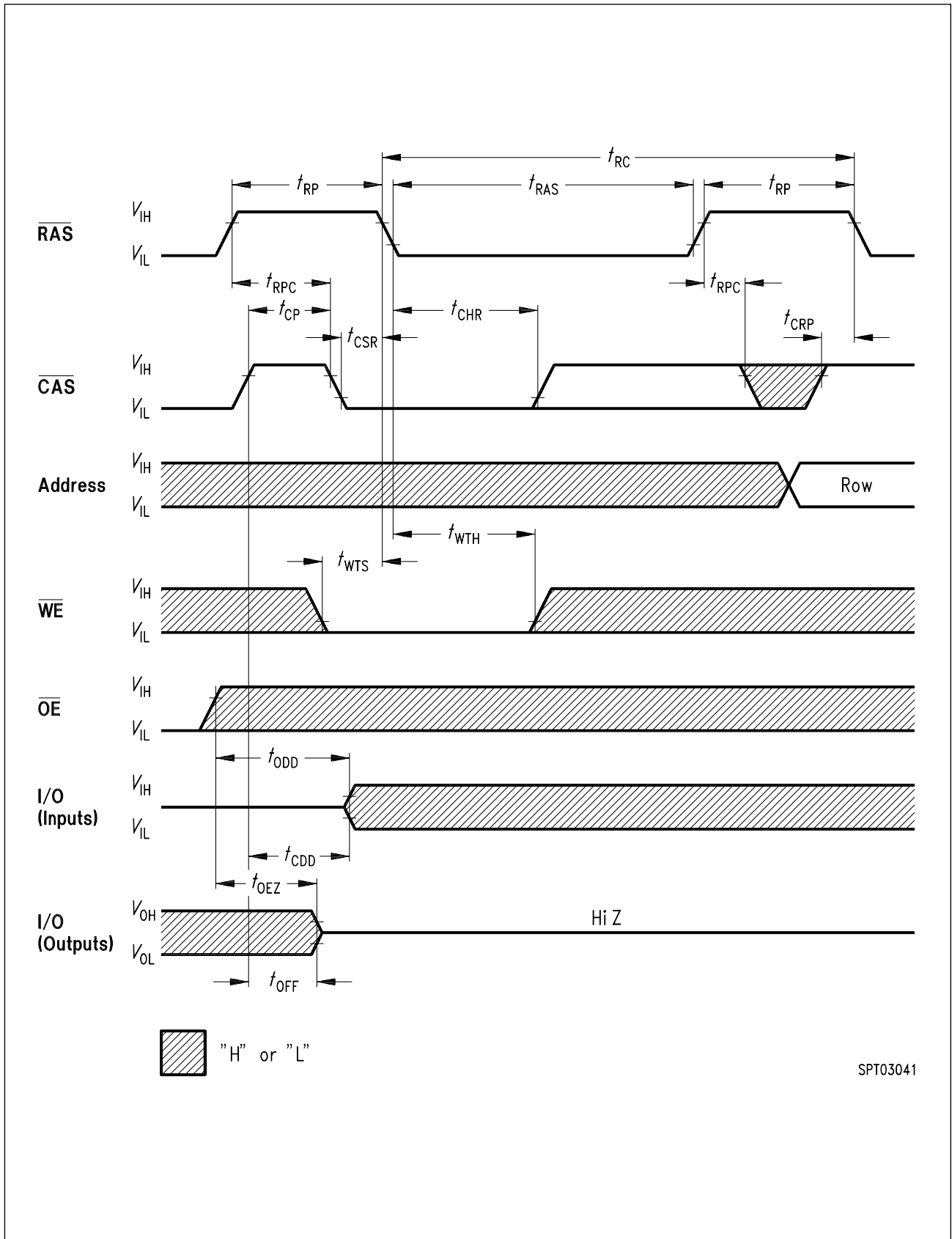


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Hidden Refresh Cycle (Early Write)



CAS-Before-RAS Refresh Counter Test Cycle



### Test Mode Entry



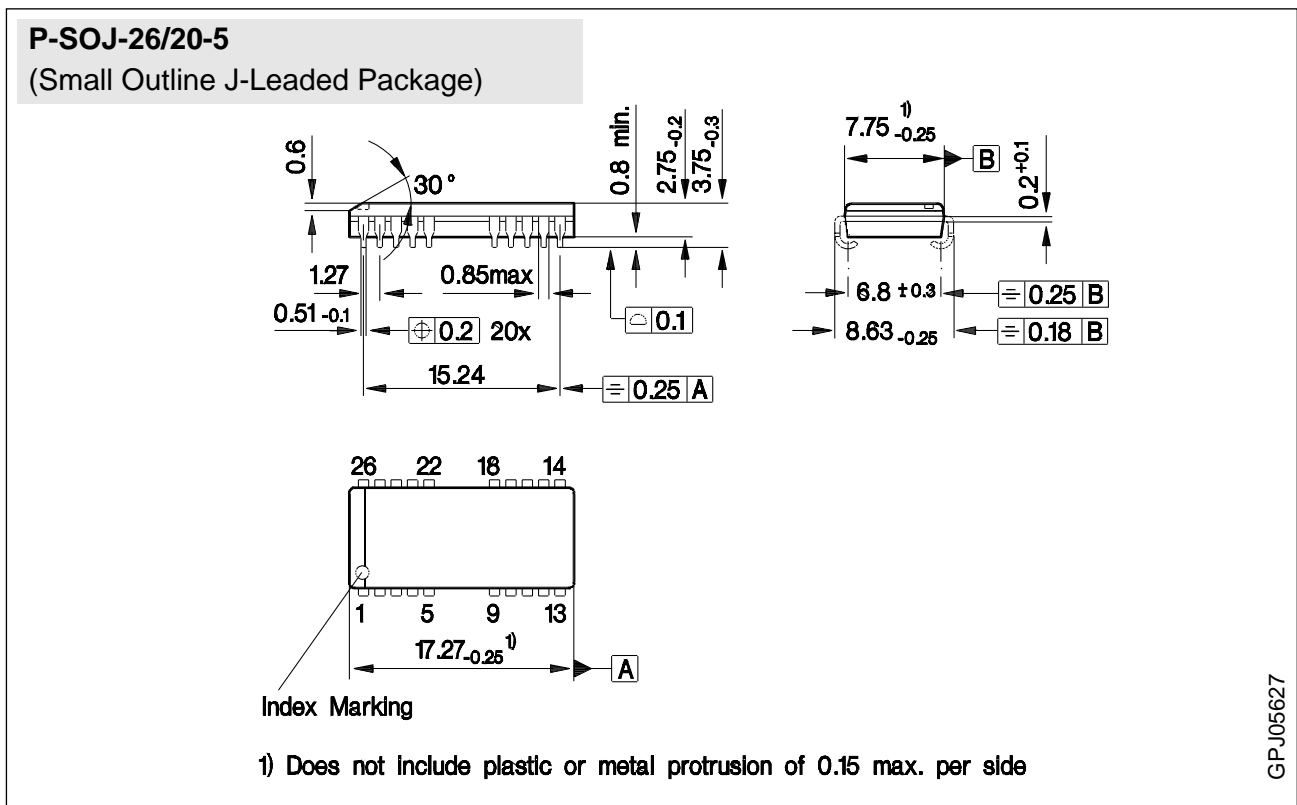
### Test Mode

As the HYB 514405BJ/BT is organized internally as 512K x 8-bits, a test mode cycle using 8:1 compression can be used to improve test time. Note that in the 1M x 4 version the test time is reduced by 1/2 for a linear test pattern.

In a test mode "write" the data from each I/O1 pin is written into eight bits simultaneously (all "1"s or all "0"s). The I/O2-I/O4 inputs are not used for writing in test mode. In test mode "read" each I/O output is used for indicating the test mode result. If the internal eight bits are equal, the I/O would indicate a "1". If they were not equal, the I/O would indicate a "0". Note that in test mode "read" I/O1-I/O3 are always driven to "ones", i.e. all outputs will be "1"s for a test mode "pass". The WCBR cycle ( $\overline{WE}$ ,  $\overline{CAS}$  before  $\overline{RAS}$ ) puts the device into test mode. To exit from test mode, a " $\overline{CAS}$  before  $\overline{RAS}$  refresh", " $\overline{RAS}$  only refresh" or "Hidden refresh" can be used.

Addresses A10R, A10C and A0C are don't care during test mode.

### Package Outlines



### Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm